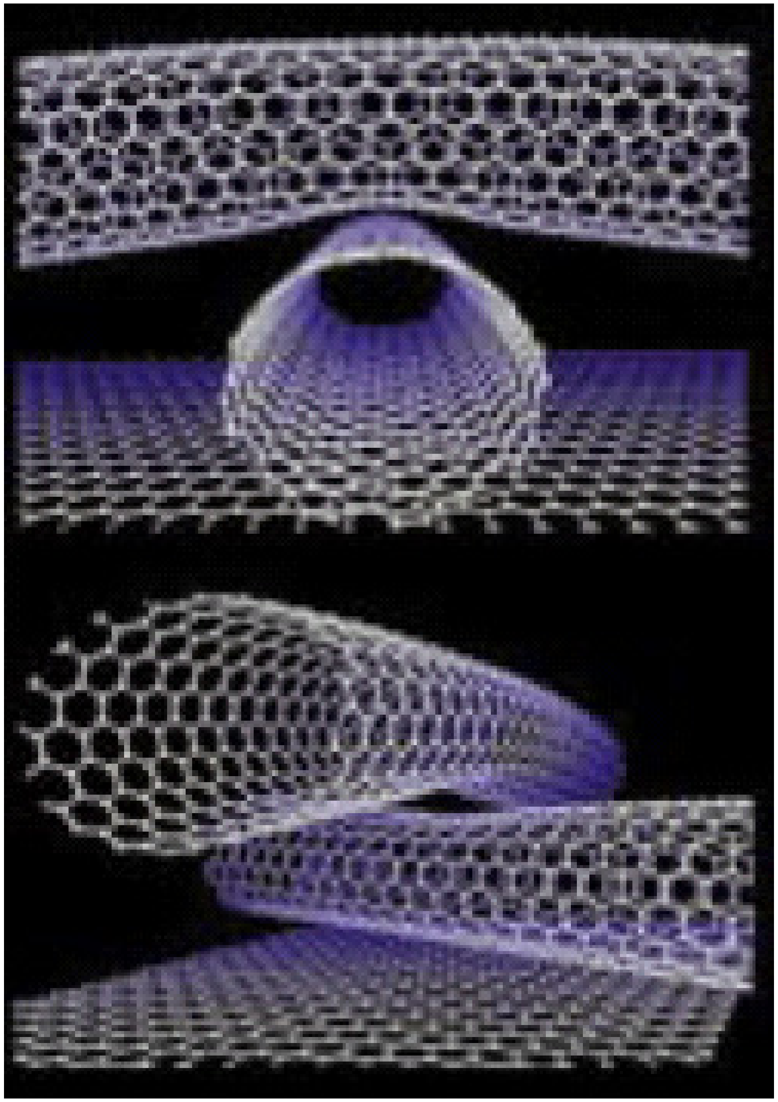
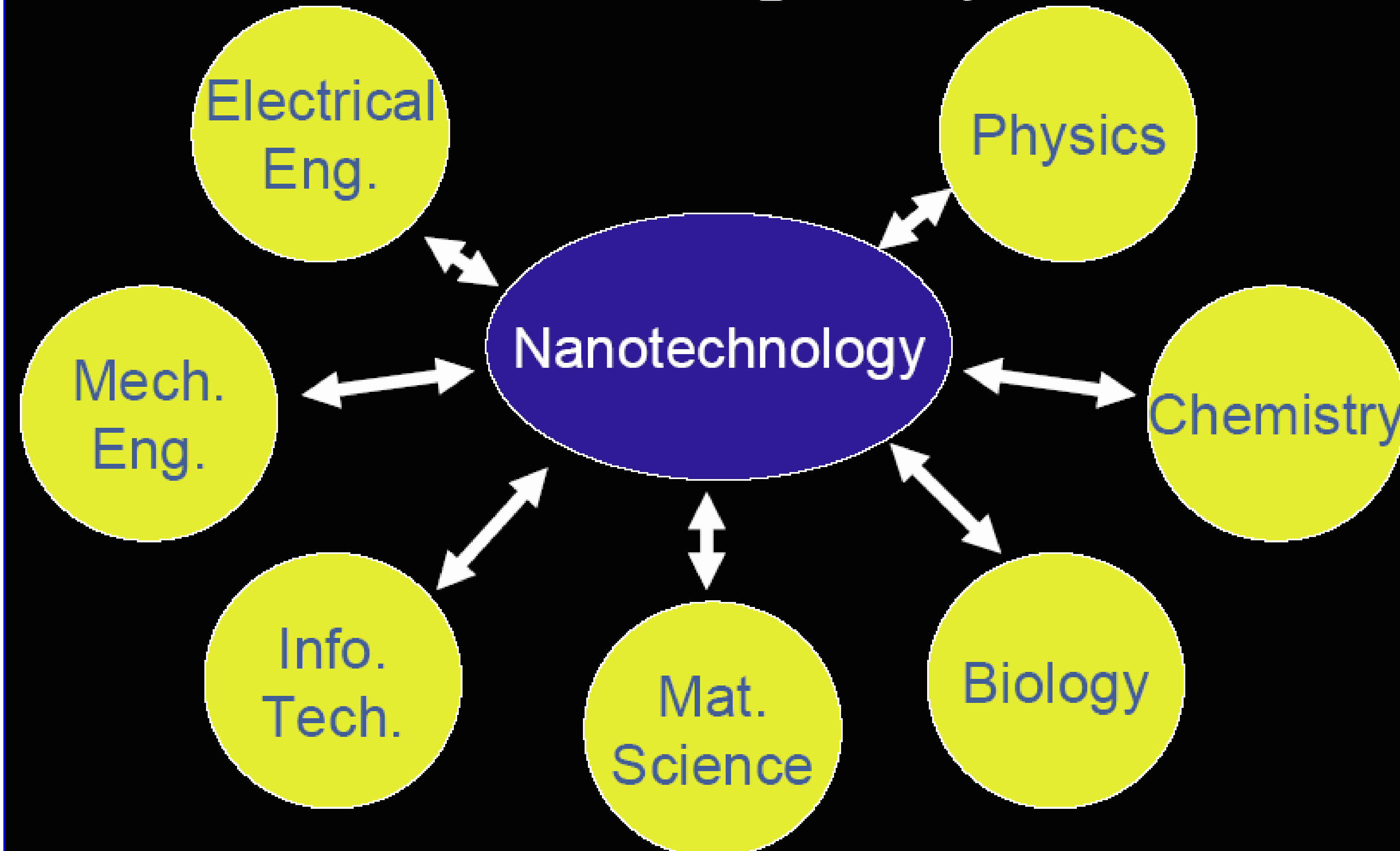
CNT BASED NANODEVICE DEVELOPMENT



Dr P K Chaudhury
Solid State Physics Laboratory
Delhi-54

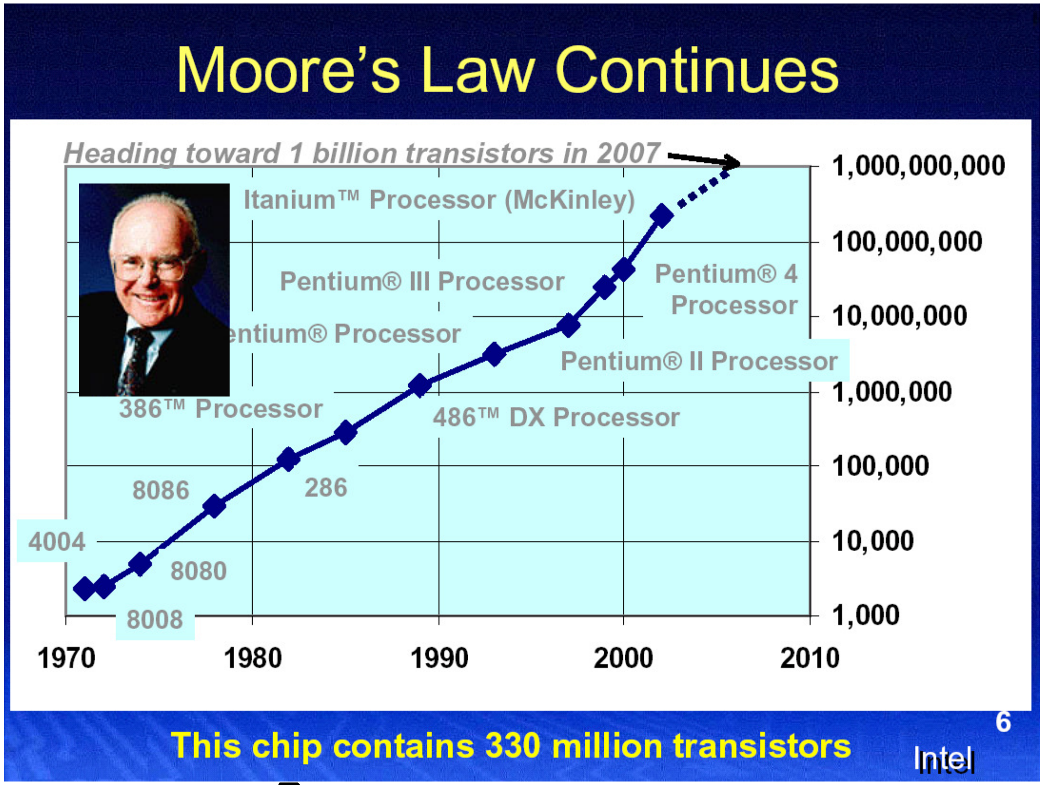
Nanotechnology is multidisciplinary:



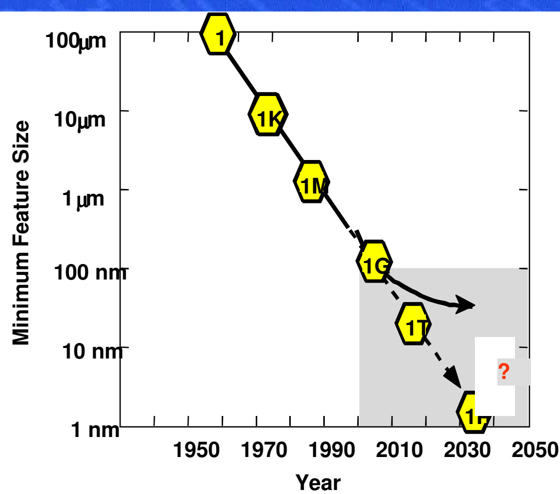
Nanotechnology/Nanoelectronics

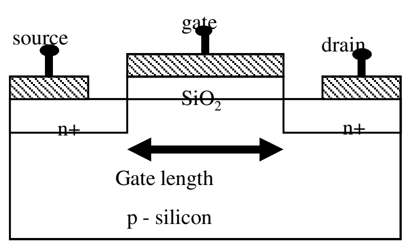
- **Nanotechnology is the design and construction** of useful technological devices whose size is a few billionths of a meter
- **Nanoscale devices** will be built of small assemblies of atoms linked together by bonds to form macro-molecules and nanostructures
- **Nanoelectronics** encompasses nanoscale circuits and devices including (but not limited to) ultra-scaled FETs, quantum SETs, RTDs, spin devices, superlattice arrays, quantum coherent devices, molecular electronic devices, carbon nanotubes, Graphene.

Moore's law and scaling theory



Moore's Law : No. of transistors on a single IC "Chip" has roughly doubled every 18months



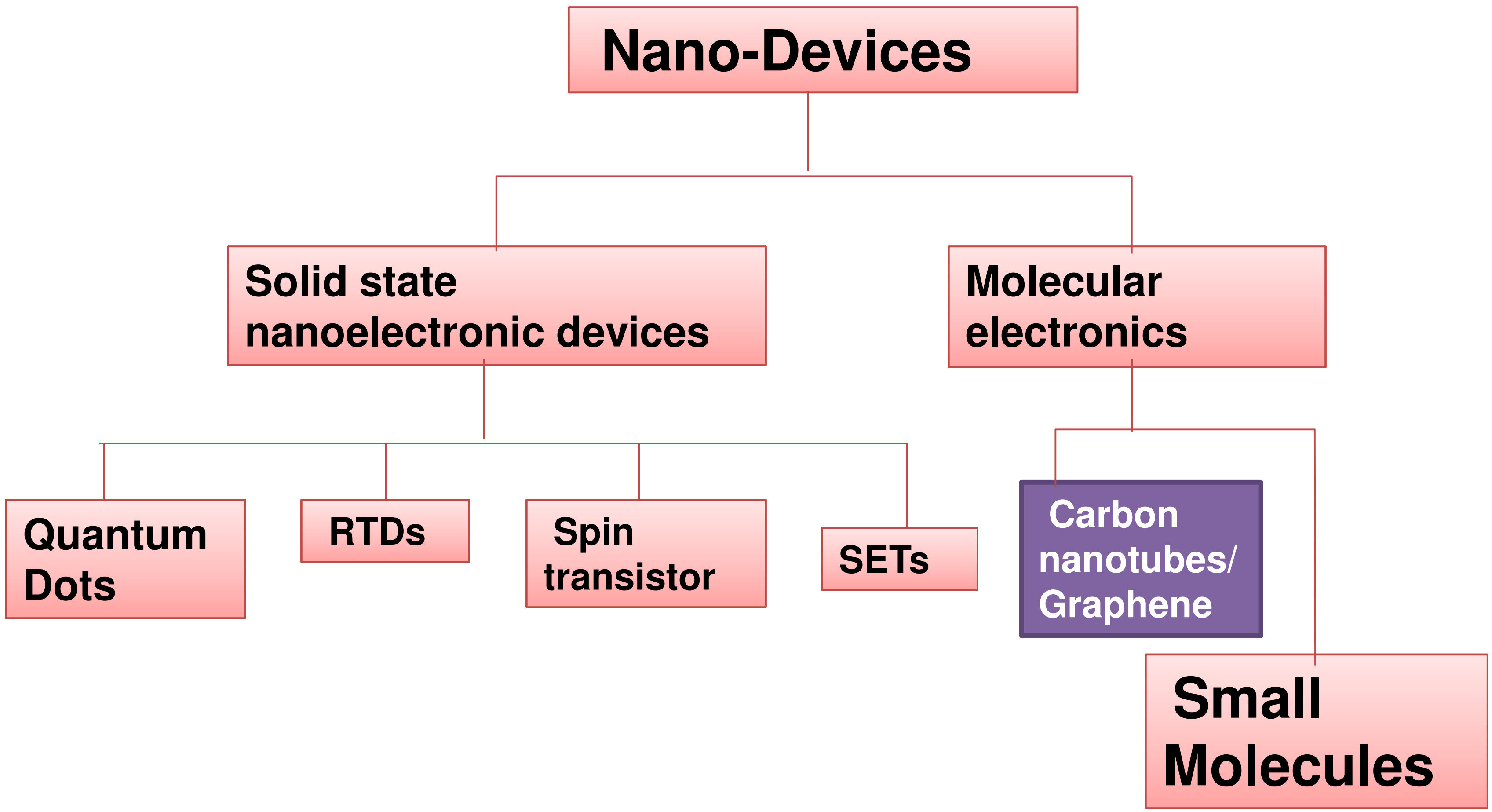


Ideal scaling:

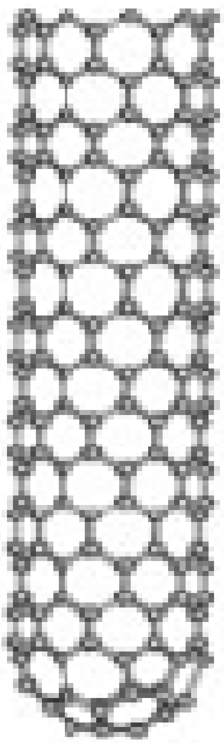
Reduce W,L by a factor of <u>a</u>
Reduce the threshold voltage and supply voltage by a factor of <u>a</u>
Increasing all of the doping levels by <u>a</u>
(W,L,tox,VDD,VTH, etc, are scaled down by a factor <u>a</u>)
For a ideal square-law device, Id is reduced by <u>a</u>, but gm and intrinsic gain Gm* ro remain the same.

As scaling into submicron region, Short Channel effects prevent further scaling.

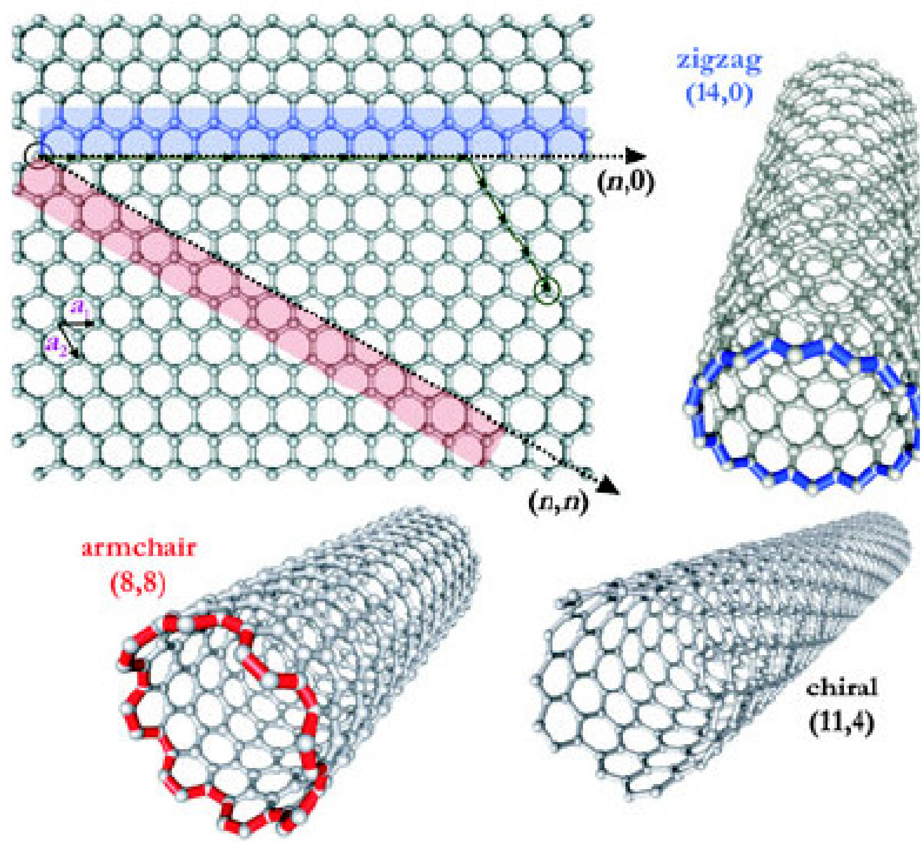
Future

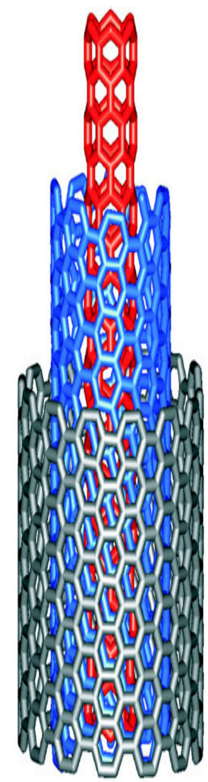

Nano-Devices
Solid state nanoelectronic devices
Molecular electronics
Quantum Dots
RTDs
Spin transistor
SETs
Carbon nanotubes/ Graphene
Small Molecules

CARBON NANO-TUBES



SWCNT

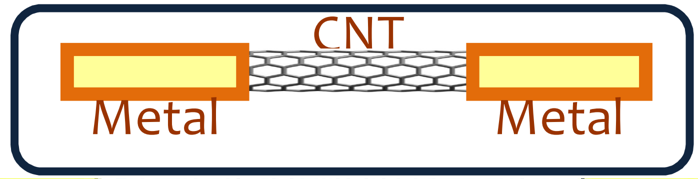


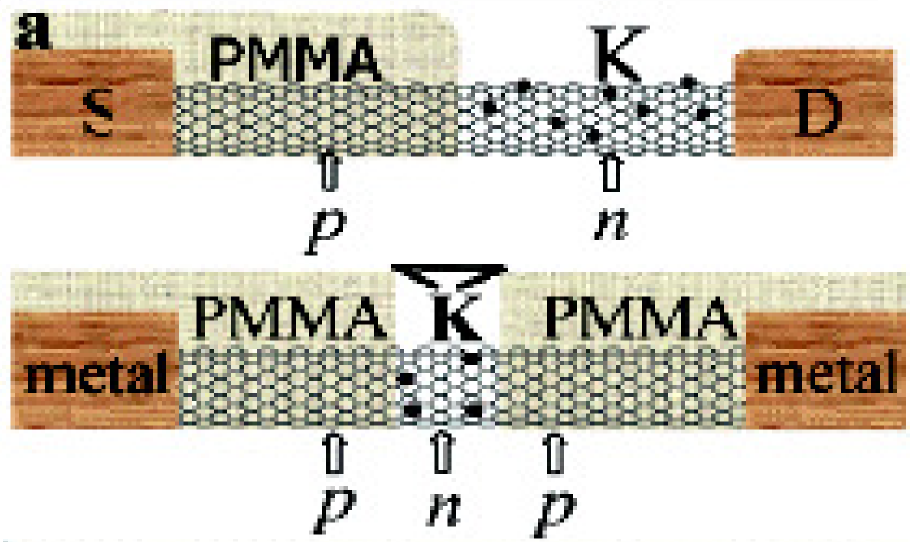


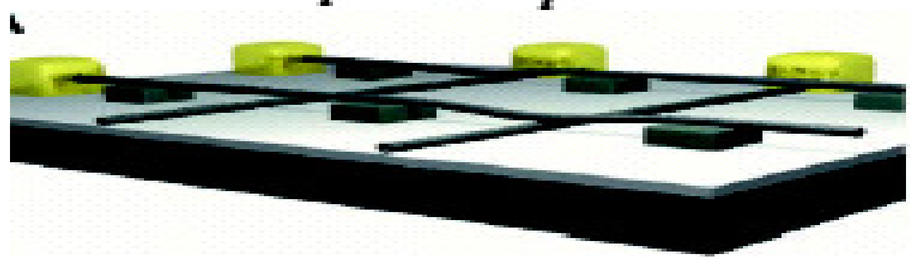
MWCNT

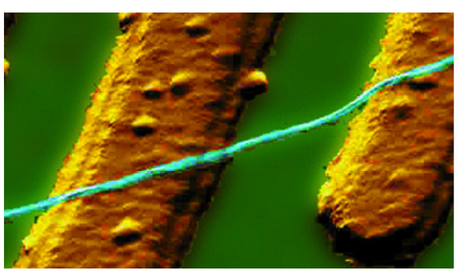
CNT BASED DEVICE

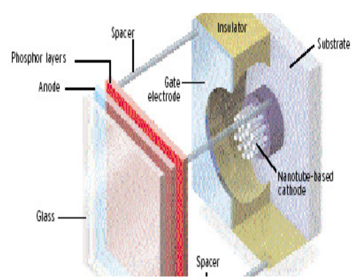
- Nano-devices
  - Resistor
  - Capacitors
  - Interconnects
  - Transistor
  - Logic Gates
  - Data Storage
  - THz Devices
  - Field Emitters
  - Sensors







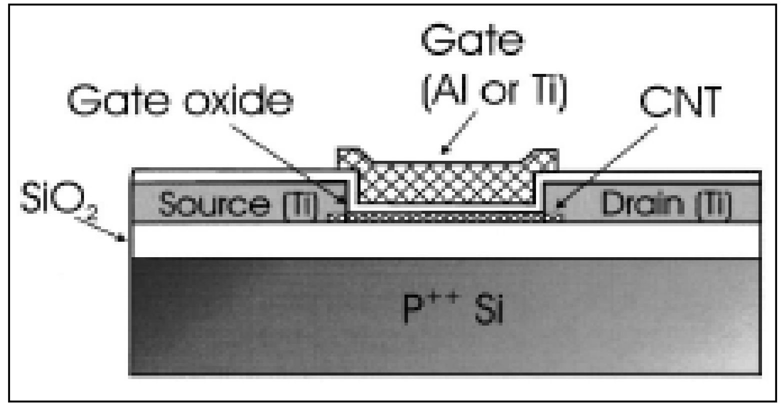


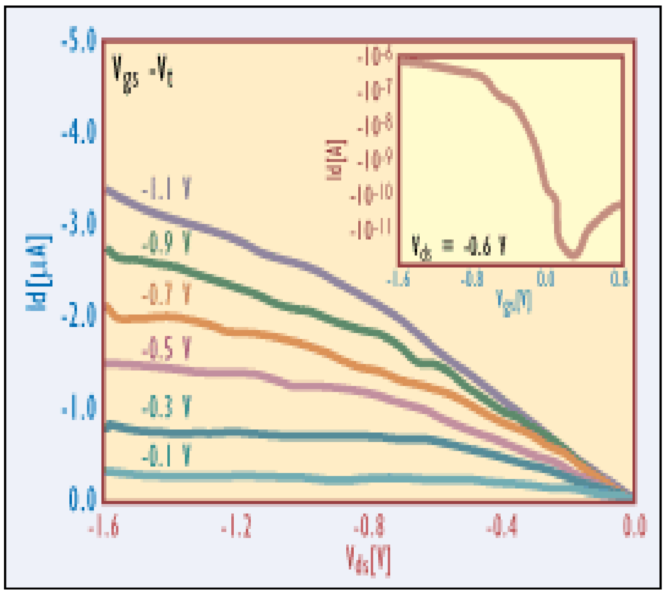


CNTFET

Front Gate FET with CNT p and n channel

Performance superior to 50 nm, 1.5nm t_{ox} MOSFET

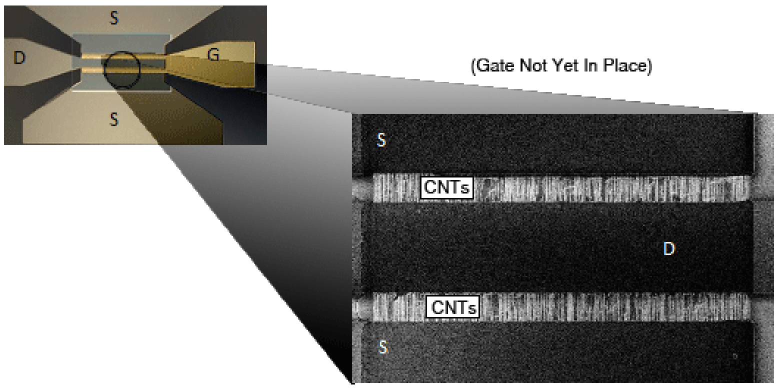


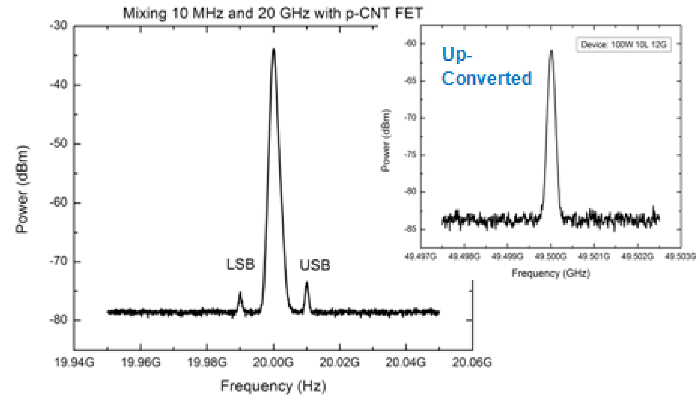


	p-type CNFET	Ref. 10	Ref. 11
Gate length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
V_t (V)	−0.5	~−0.1	~−0.2
I_{ON} (μA/μm) ($V_{ds}=V_{gs}-V_t \approx -1$ V)	2100	265	650
I_{OFF} (nA/μm)	150	<500	9
Subthreshold slope (mV/dec)	130	~100	70
Transconductance (μS/μm)	2321	975	650

Wind et al (IBM), APL May 2002

HIGH SPEED APPLICATIONS

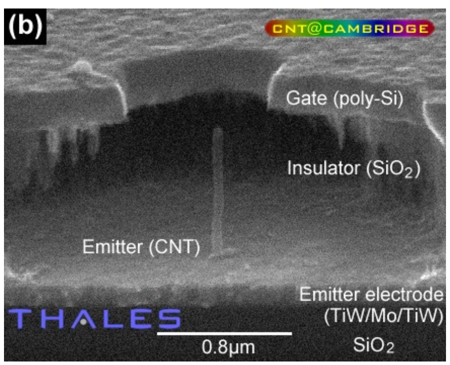




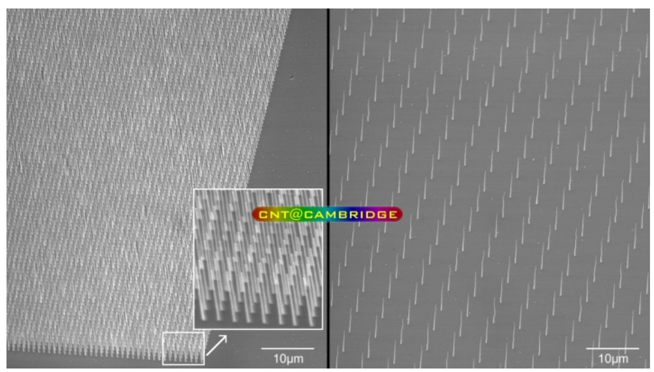
The HF capability of these devices seems to be well beyond 50 GHz.

Parallel-CNT Field Effect Transistors for High Speed Applications

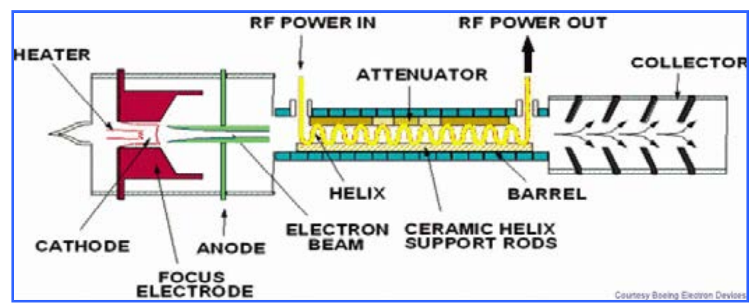
COLD CATHODE FIELD EMITTERS



Carbon Nanotube Electron Guns for Nanolithography (EC project NANOLITH)

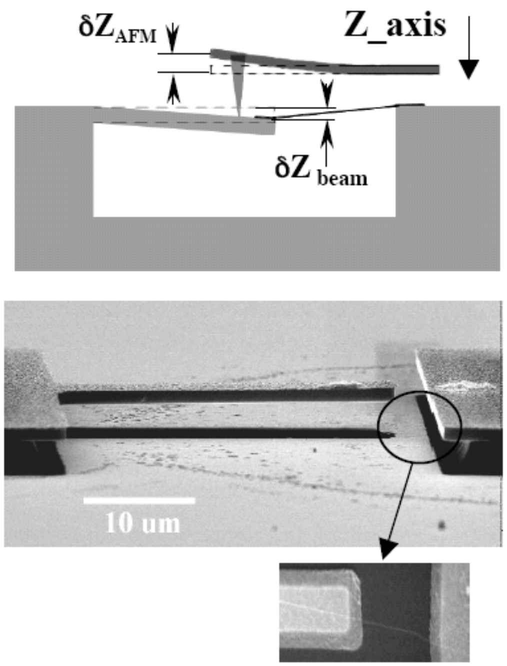


Carbon Nanotube Electron Guns

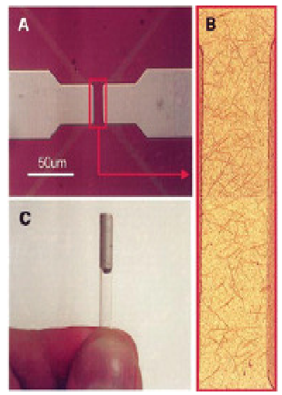


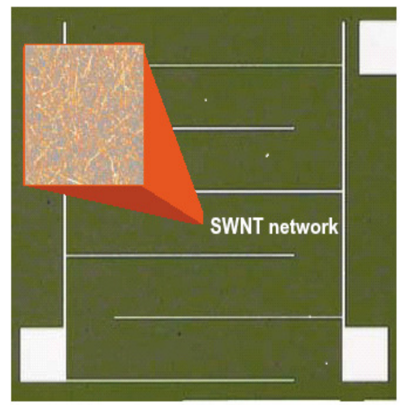
Traveling Wave Tube

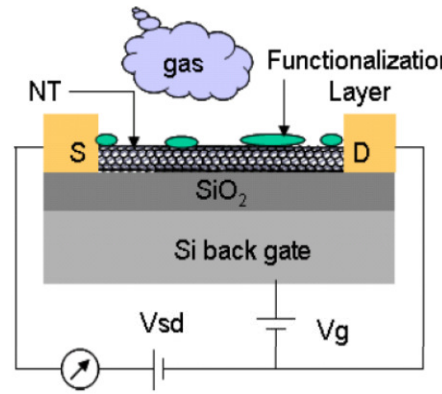
CNT BASED SENSORS

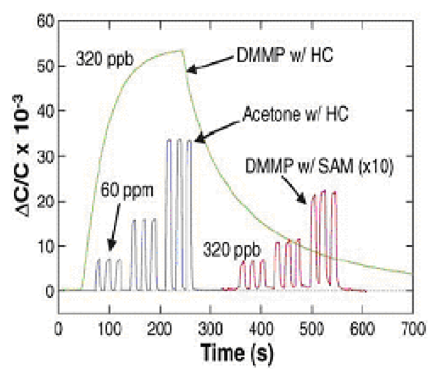


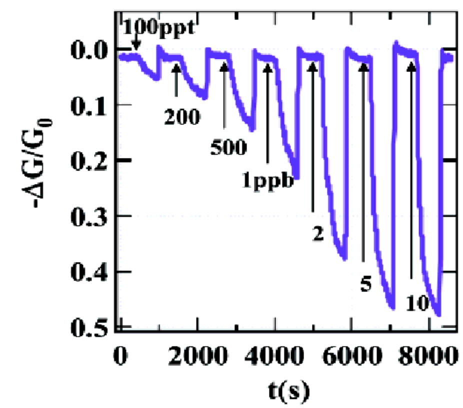
Strain of less than 1% results in the CNT changing from metal to semiconductor.







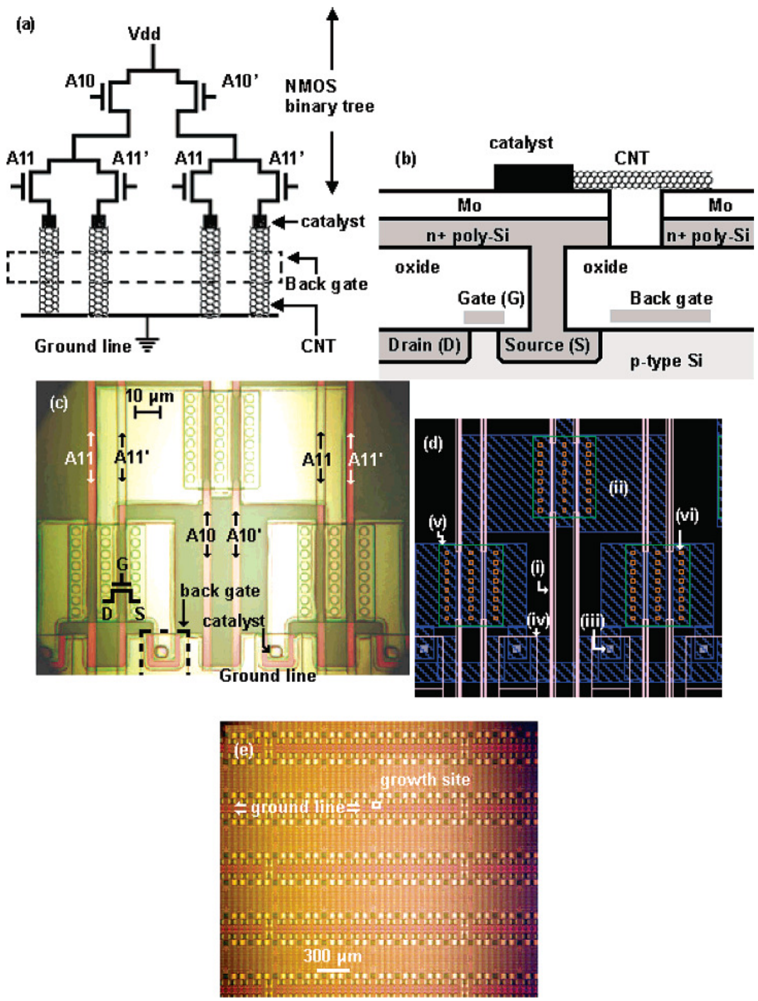




PHYSICAL SENSORS

CHEMICAL SENSORS

Monolithic Integration of Carbon Nanotube Devices with Silicon MOS Technology



An integrated circuit combining single-walled carbon nanotube (SWNT) devices with n-channel metal oxide semiconductor (NMOS) field effect transistors has been demonstrated at *University of California*. Shows many possibilities, including electronically addressable nanotube chemical sensor arrays.

Challenges

•Although CNT devices and interconnects separately have been shown to be promising in their own respects, there have been few efforts to combine them in a realistic circuit

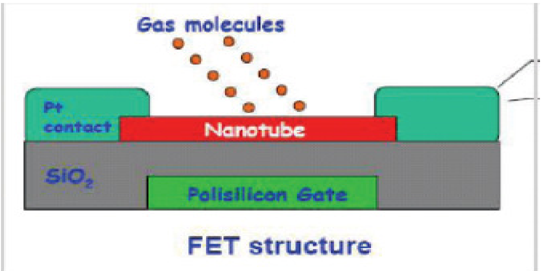
•Several process-related challenges need to be addressed before CNT-based devices and interconnects can enter mainstream VLSI manufacturing

•Problems include purification, separation, control over length, chirality and desired alignment, low thermal budget and high contact resistance

Present Interest @ sspl

Development of Enabling Technologies for Carbon Nanotube Based Sensors

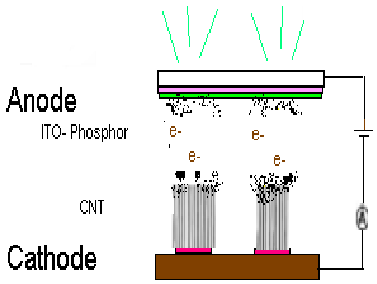
* **Enabling Technologies**
  SWNT Growth, Purification & Functionalization
* **Prototypes for Testing**
  CNT Resistor & FET Sensor Elements



CNT based gas-sensor

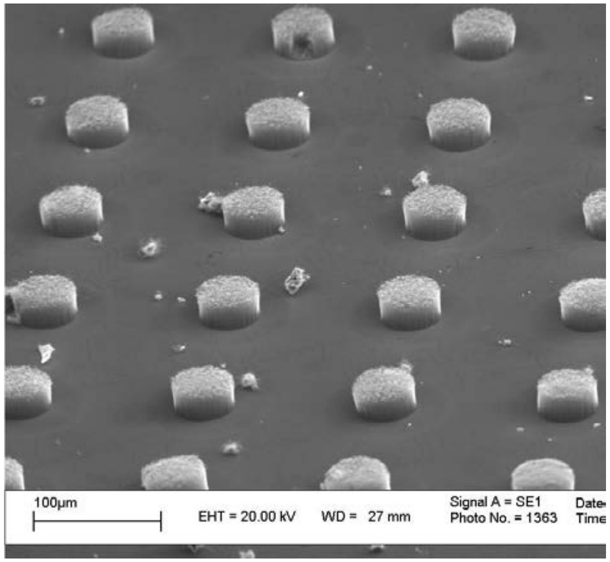
Development of CNT based Electron Emitter for Vacuum Microelectronics Devices

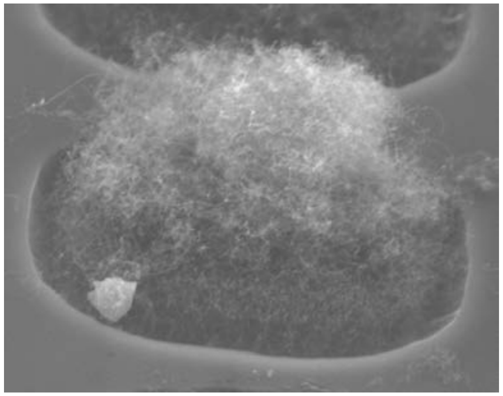
- **CNT type FE Arrays for external grid**
- **CNT type FE Arrays with integrated grid**

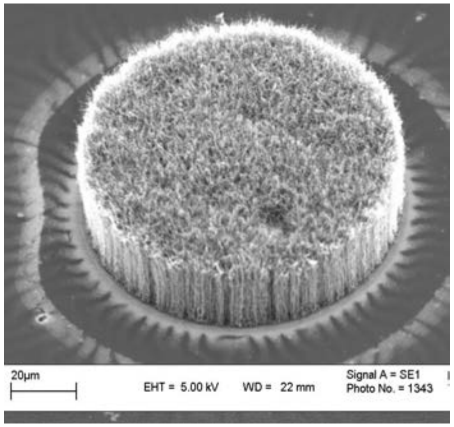


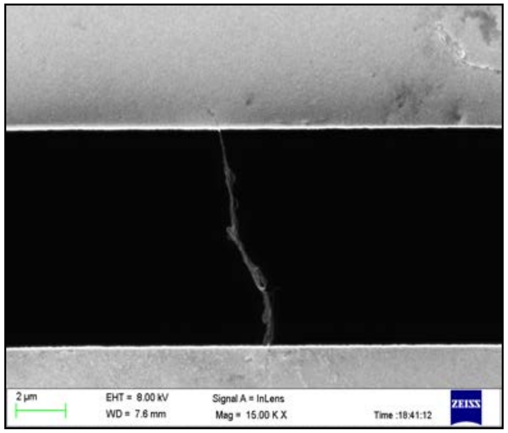
CNT GROWTH FOR DEVICES

- Selective and controlled Growth
- Aligned Growth
    - Vertically aligned to surface
    - Horizontally aligned
- Lower Growth Temperature

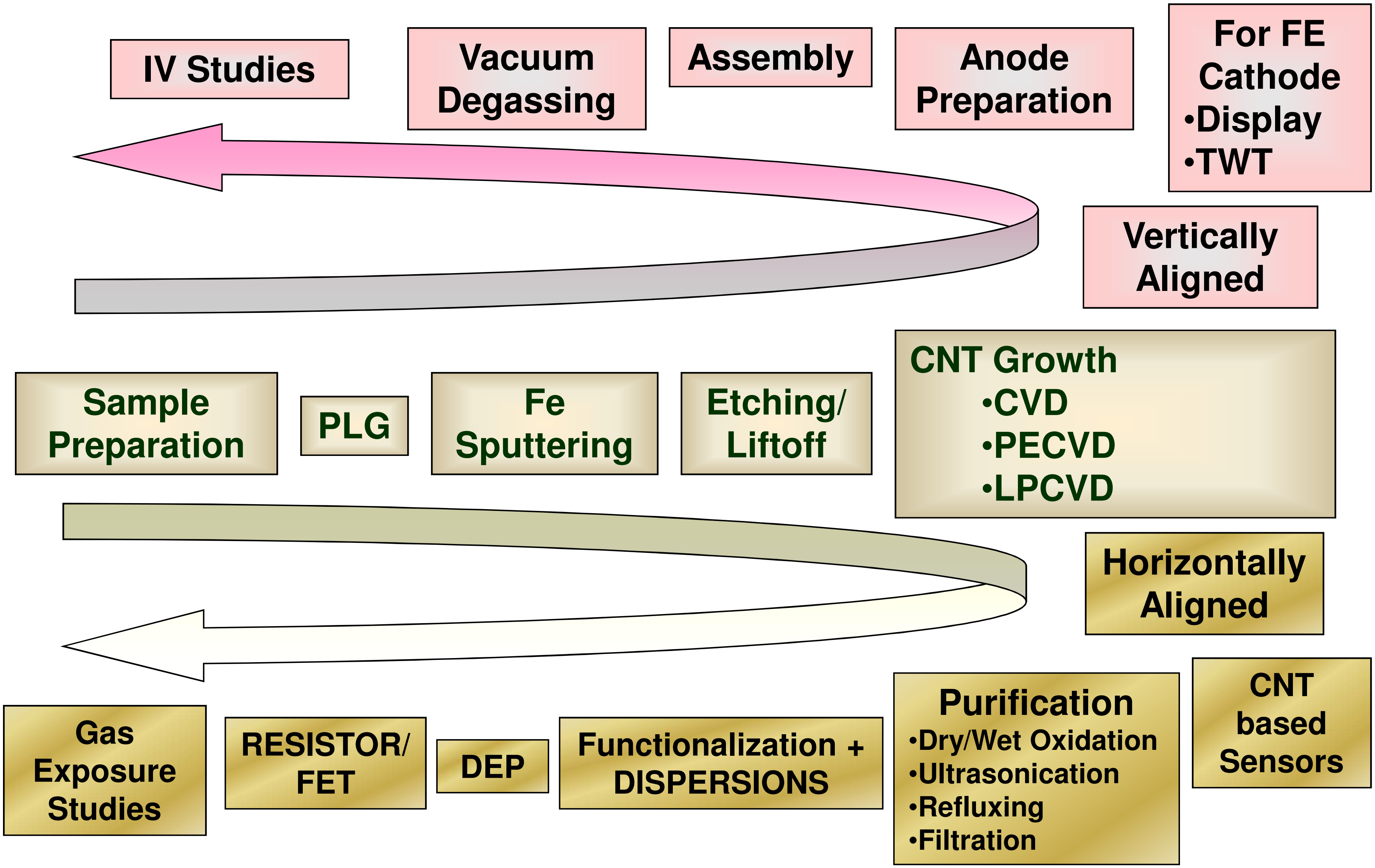








Activity Flow Diagram



CNT Growth Setups: SSPL made

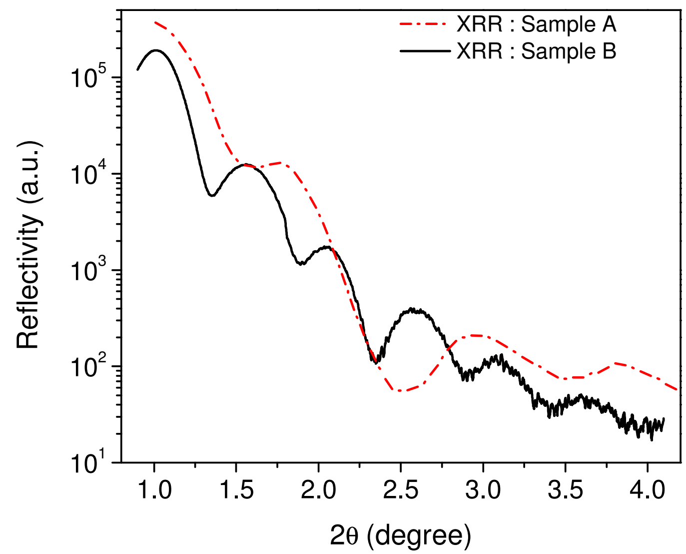
LPCVD System

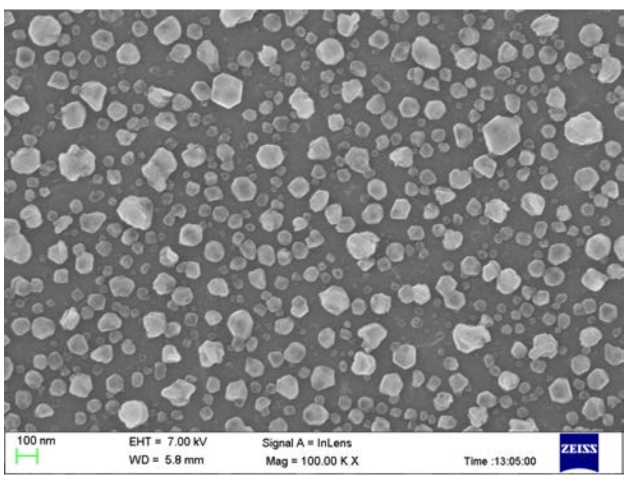
CVD System

PECVD System

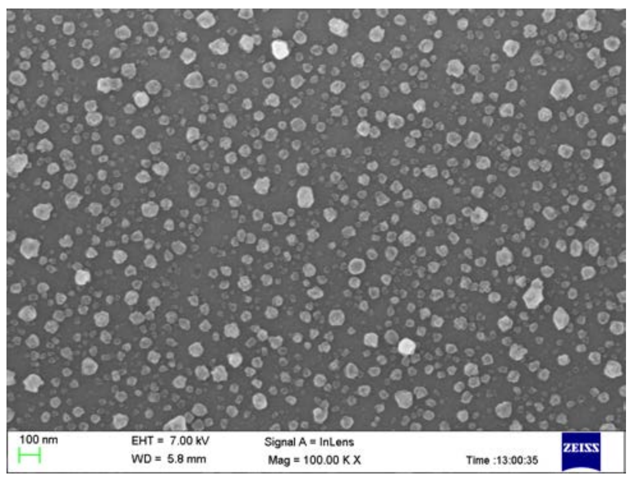
Analysis of Catalyst film

- Surface roughness ~ 0.65nm -0.90 nm
- The Fe-particle size reduces with thickness of the Fe Film
- The particle size is from few nanometer to 30 nm in 2 nm film
- The particle size is from 10-50 nm in 4 nm film
- The particle size is from 20-100 nm in 8 nm film

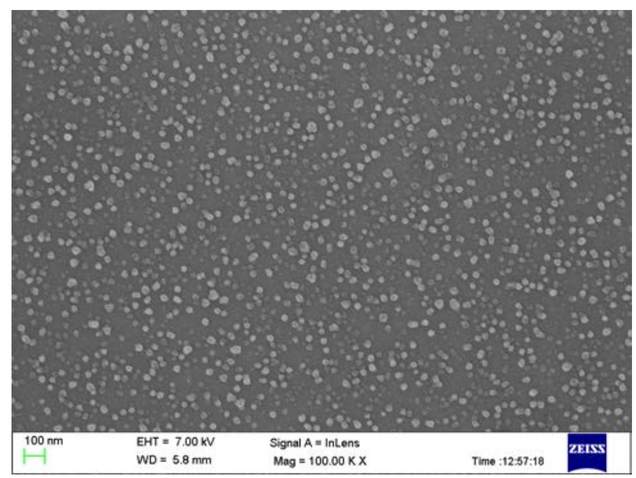




Fe-8 nm

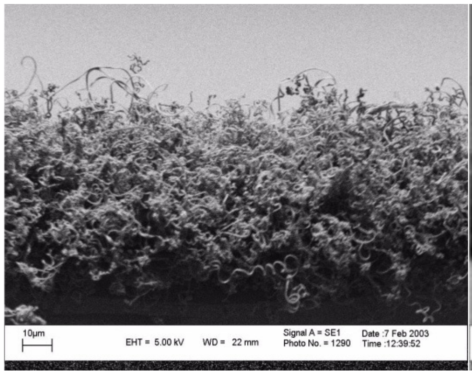


Fe- 4 nm

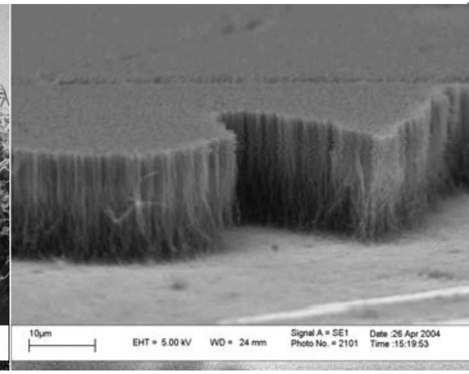


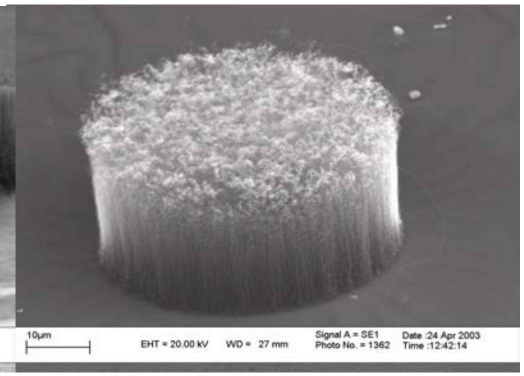
Fe-2 nm

Carbon Nanotube SEM Images:CVD

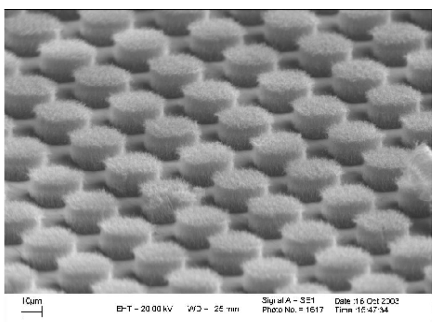


Unaligned CNT growth

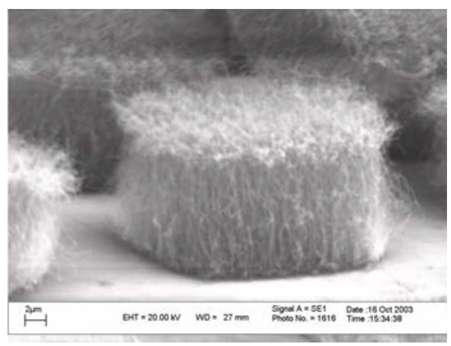




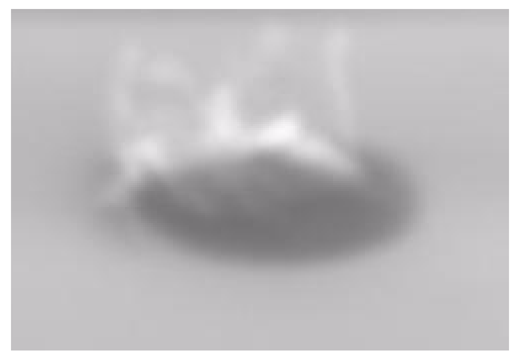
Selective and Vertically Aligned Growth



Array of 50 micron dots

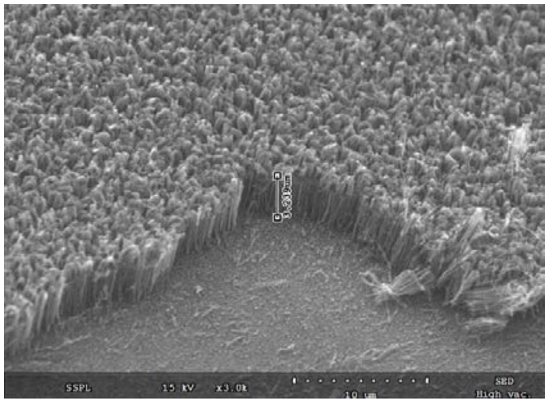


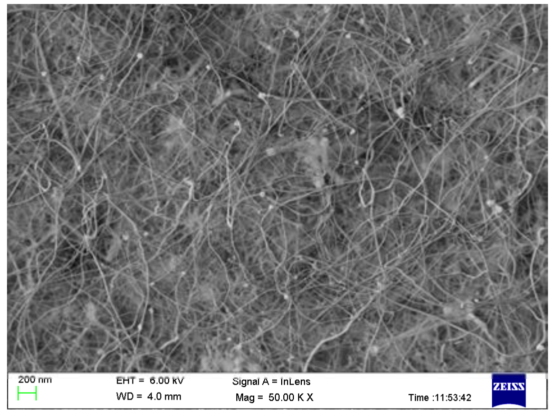
50 micron dot

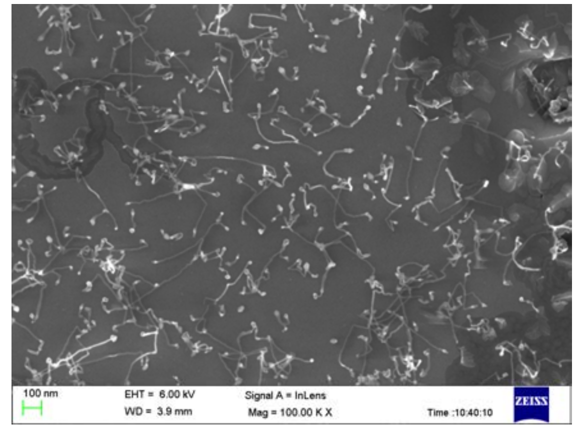


CNT on 1 micron dot

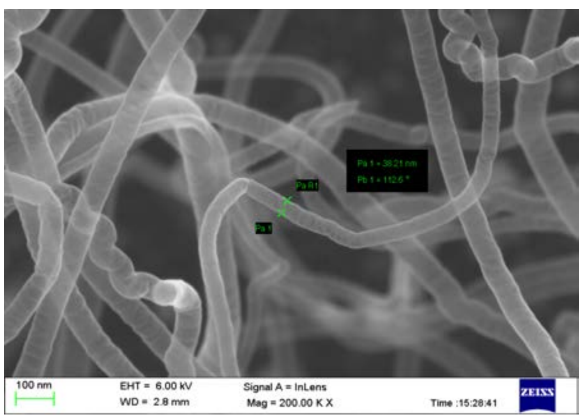
LPCVD GROWTH

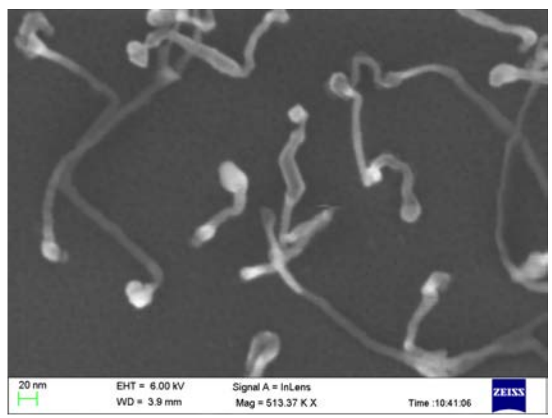


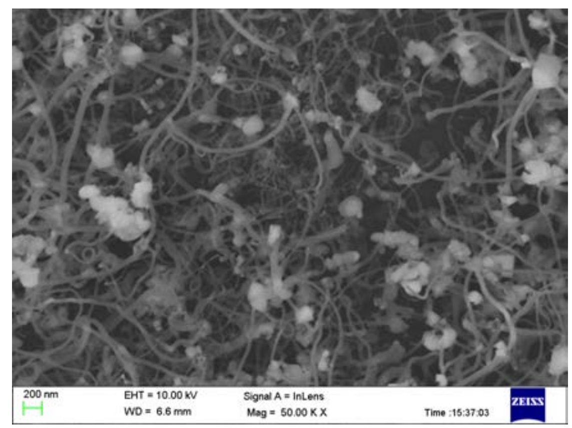




Growth Parameter : 1000^oC, H_2@1 SLM, NH_3@ 0.5 slm, CH_4 0.2 SLM, T=30 min







Growth Parameter : 1000 ^oC, H_2@1 SLM, N_2@ 1 SLM, CH_4@.5 SLM, T=10 min

Fe-2nm

Field Emitter Arrays (FEA) / Cold Cathodes

Field Emitter Arrays (FEA)

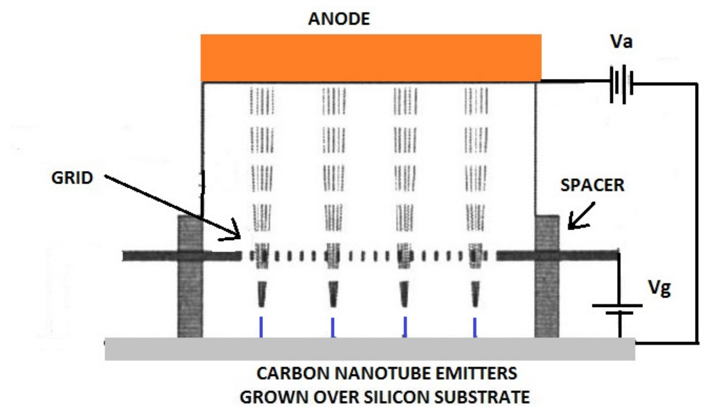
- ❖ Carbon Nanotubes based FEA
- ❖ Cathode of 1 cm diameter
- ❖ 100 mA Emission Current
- ❖ 5000 Hours of Life

External Grid Approach

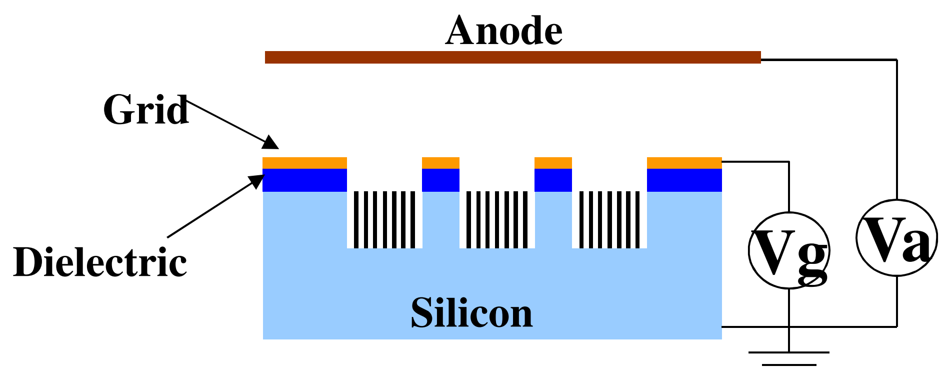
- FEAs on Planar substrate
- External Grid to be mounted separately

Integrated Grid Cathode

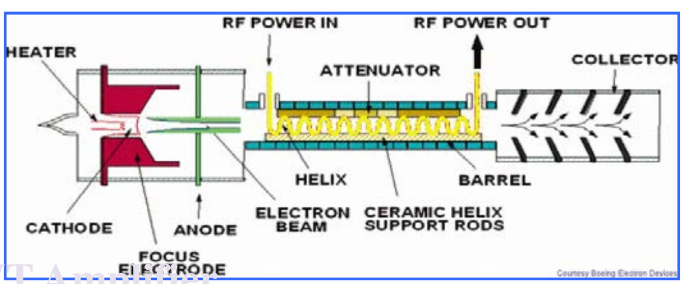
- CNT growth inside silicon Pits
- Integrated thin-film Grid



Cold Cathode with External Grid

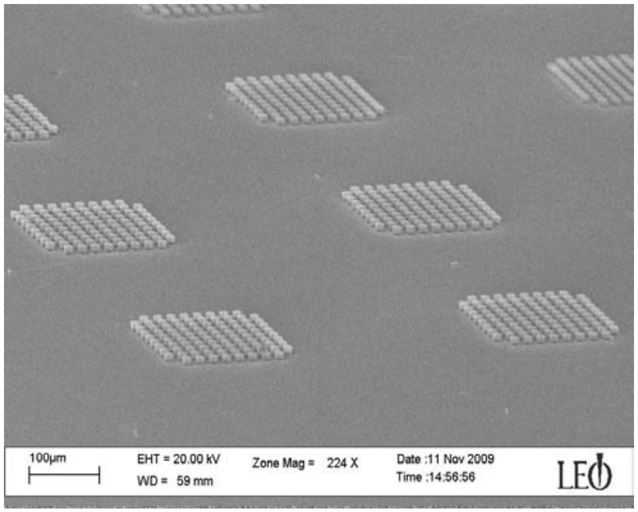


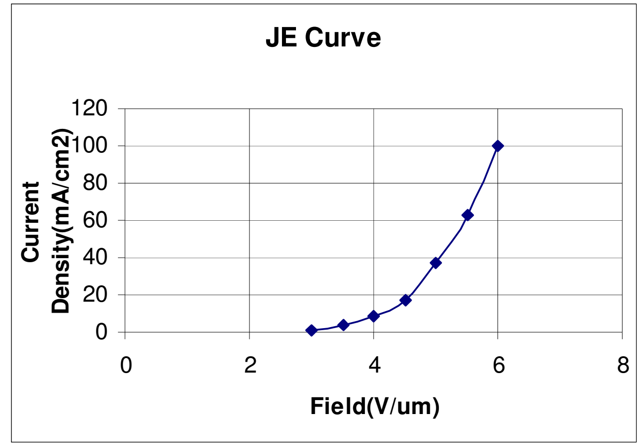
Cold Cathode with Integrated Grid



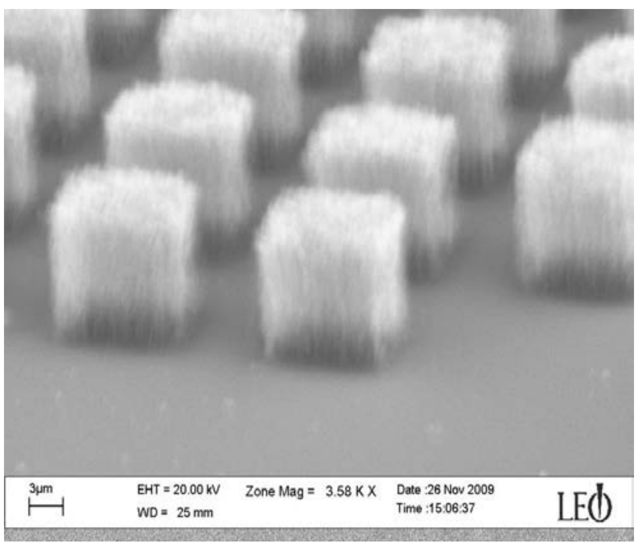
TWT Amplifier

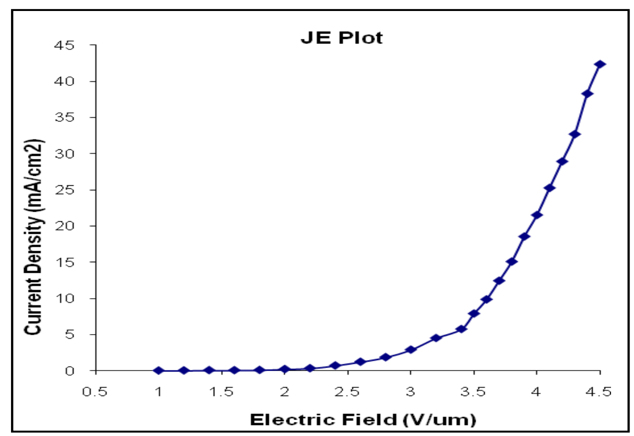
Field Emitter Arrays (FEA) / Cold Cathodes





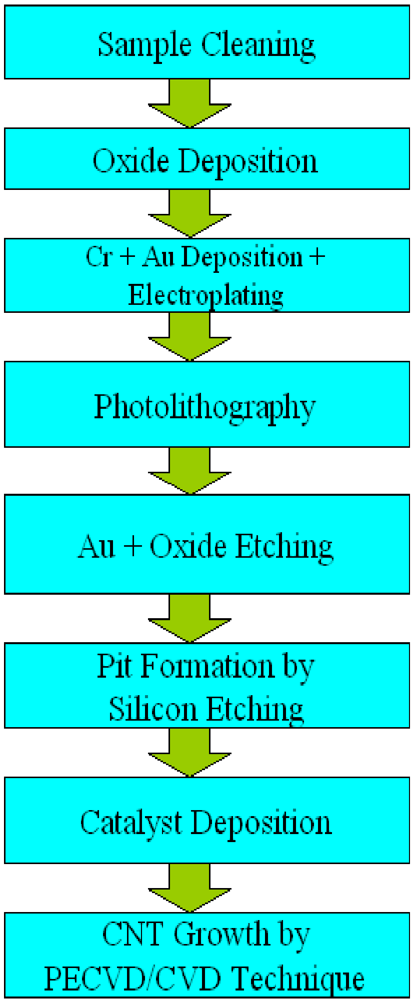
100 mA/cm2 Current Density @6 volts/micron

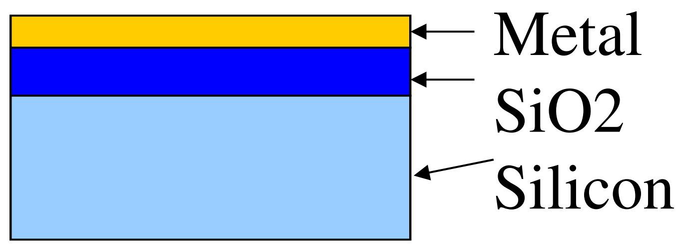


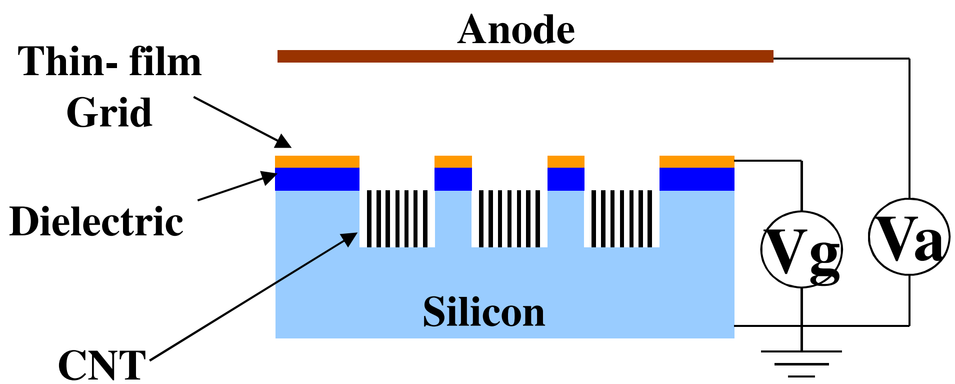


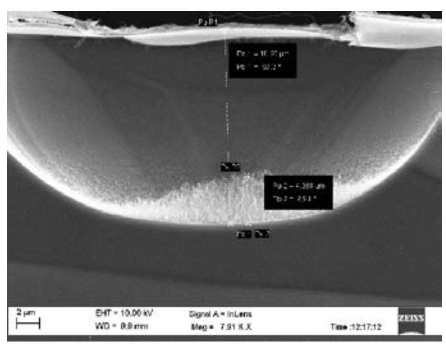
5um x 5 um CNT dot with 20 µm spacing

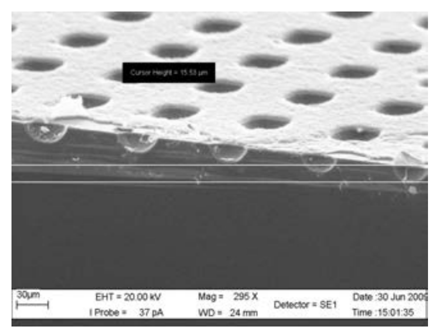
Fabrication of Cathodes With Integrated Grid

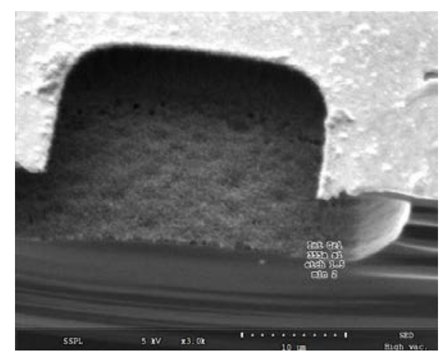










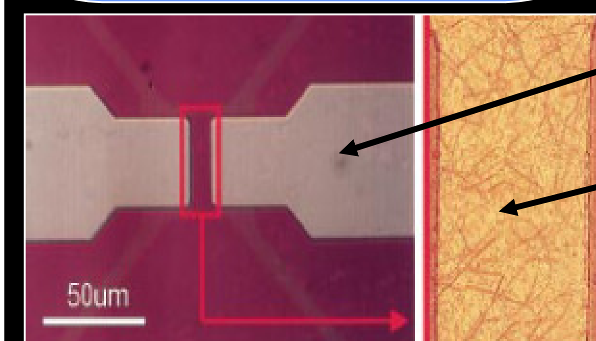


Process Steps Involved

CNT Sensors : Two Approaches

EX-SITU

- Grow CNT in powder form
- Purify CNT then Disperse & Functionalize them
- Pattern Contacts on a substrate
- Spread CNT between Contacts



PRINCIPLE

Conductance Change

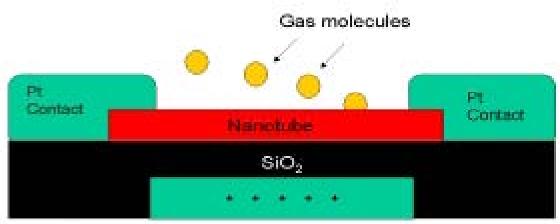
DEVICE

CNT-Resistor

CNT-FET

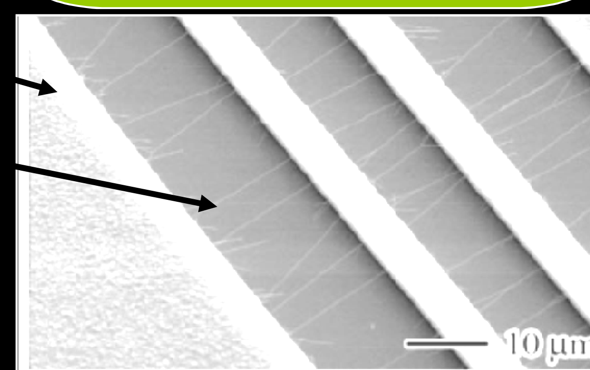
Contacts

CNT



IN-SITU

- Prepare contacts on substrate
- Deposit Catalyst over contacts
- Directly grow CNT between two contacts
- Functionalize CNT



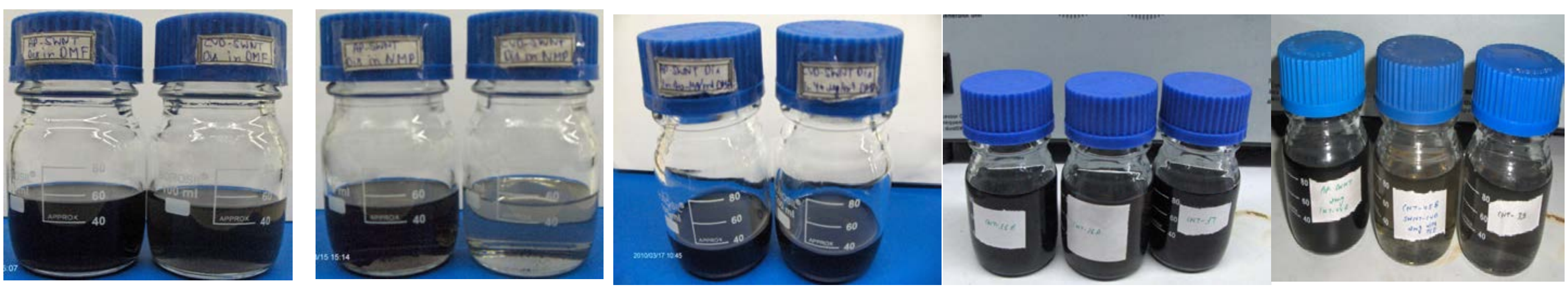
CNT Purification And Dispersions

CNT Purification

- Impurities: Amorphous Carbon & Catalyst
- Developed multi-step purification method
- Reducing metal content from ~ 34% to ~1%

CNT Dispersions

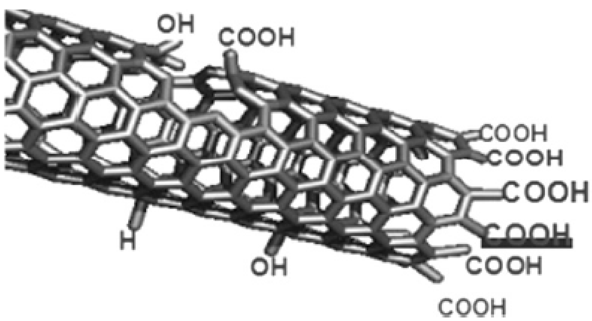
- Media
  - Aqueous (Using SDS surfactant)
  - Organic
    - Dimethyl formamide (best)
    - Dichloromethane
    - Trichloroethylene
    - N-methyl pyrrolidine
    - Dimethyle acetamide
- Concentration
  - 50 mg/ml, 200 mg/ml, 800 mg/ml

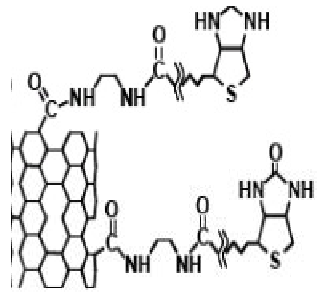


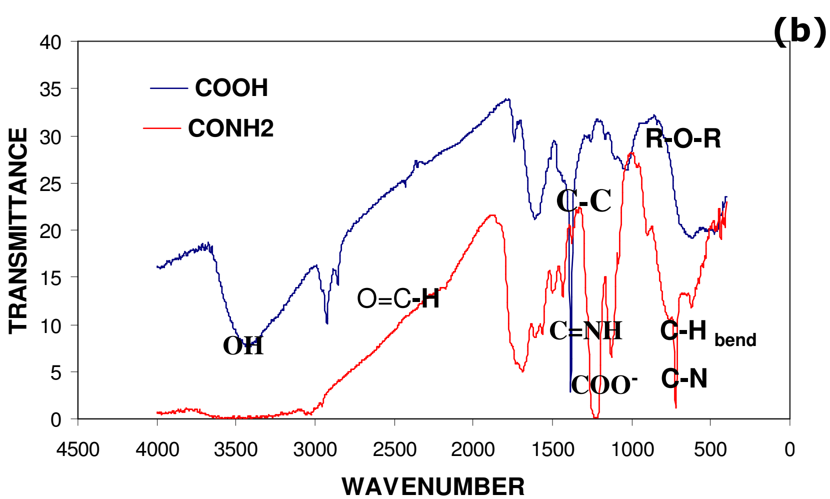
DMF NMP In DMA In DCM In TCE

SWNT Functionalization & Characterization

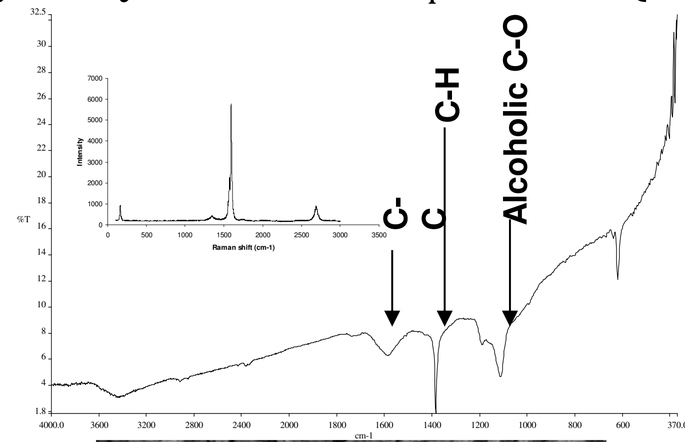
- **Carboxylation using mixture of HNO_3 and H_2SO_4**
- **Amidation with Thionyl Chloride and Ethylene Diamine**
- **Hydroxylation with $KMnO_4$: TPABr (PTC)**

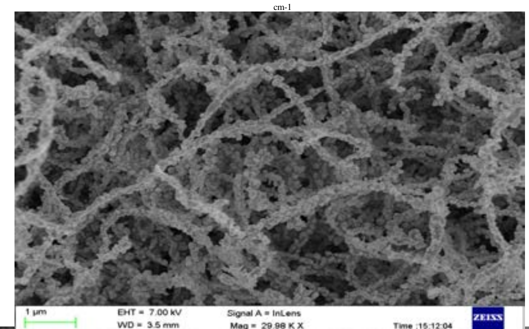


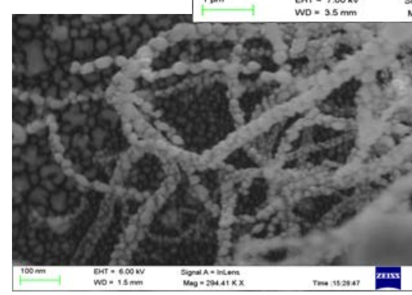


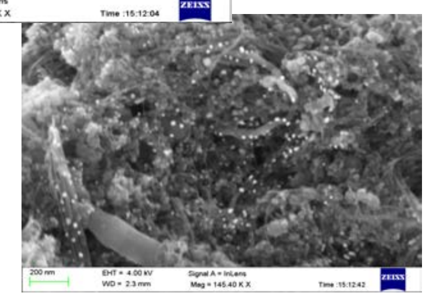


Hydroxylation $KMnO_4$: TPABr (PTC)



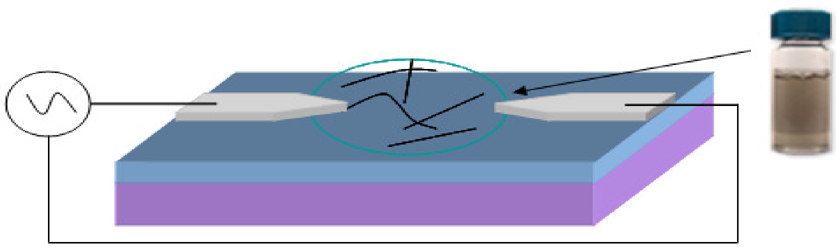


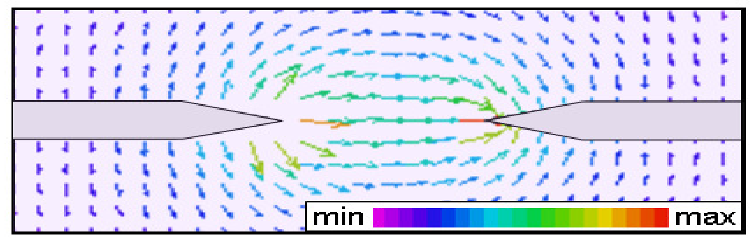


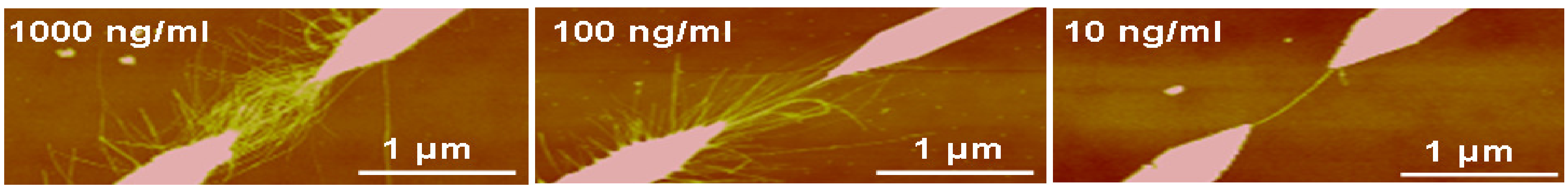


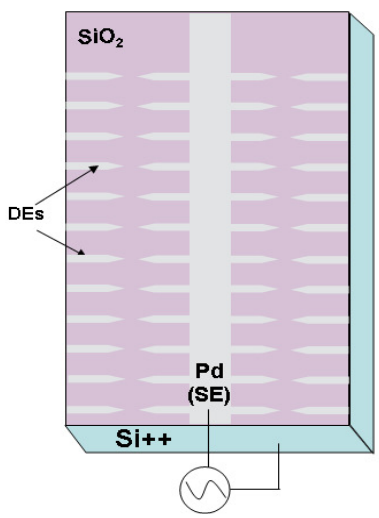
Au & Pd Decorated CNT'S

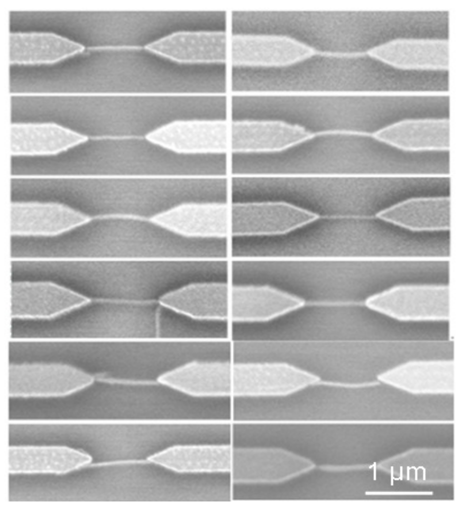
Dielectrophoretic Assembly of individual CNT devices (design)





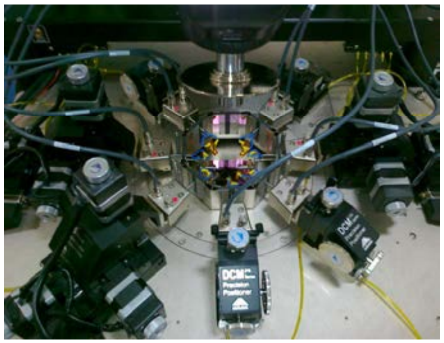
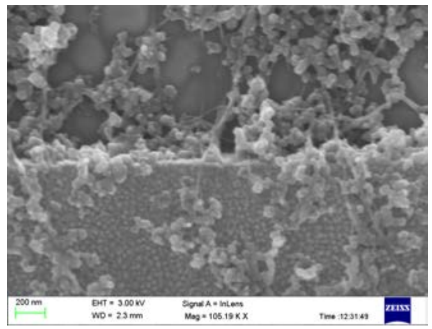
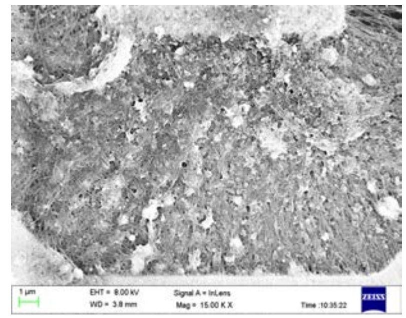
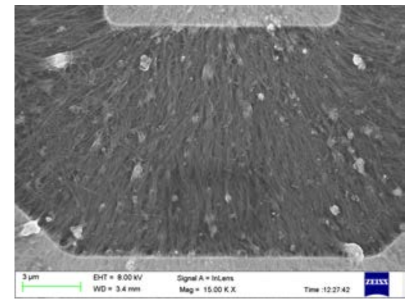
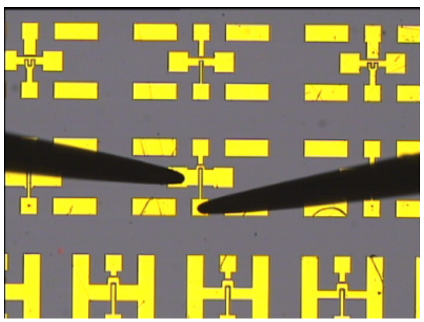
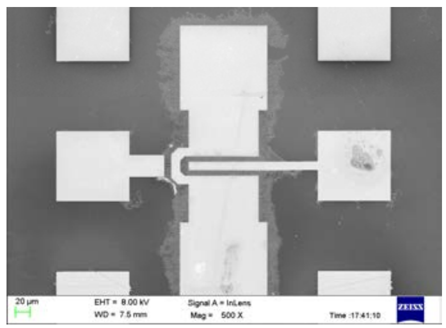
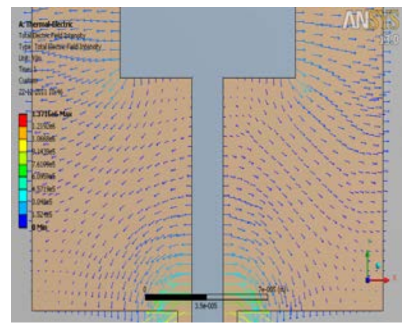
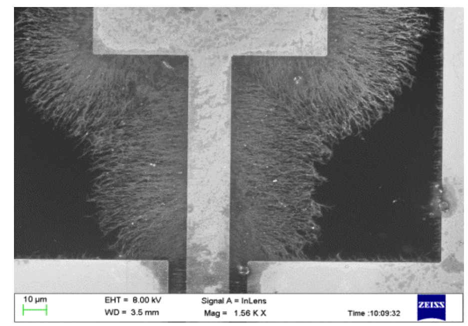
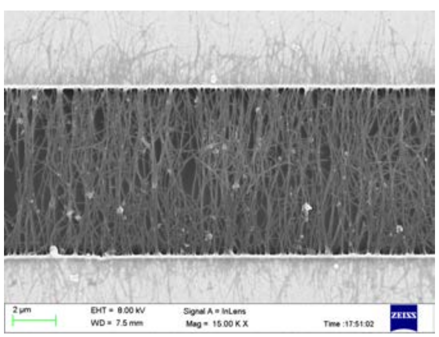
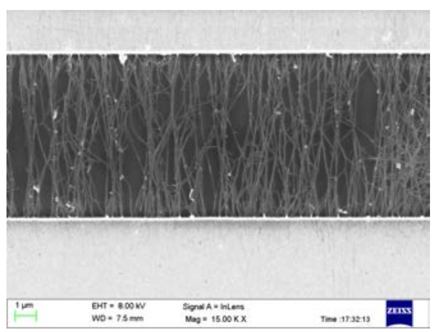
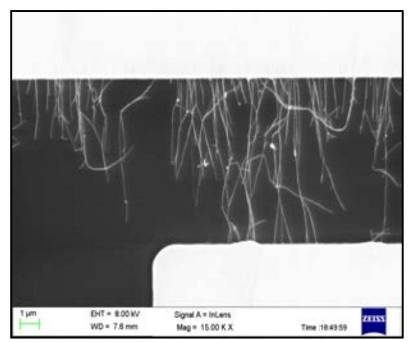
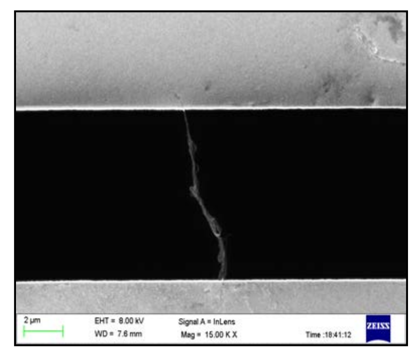




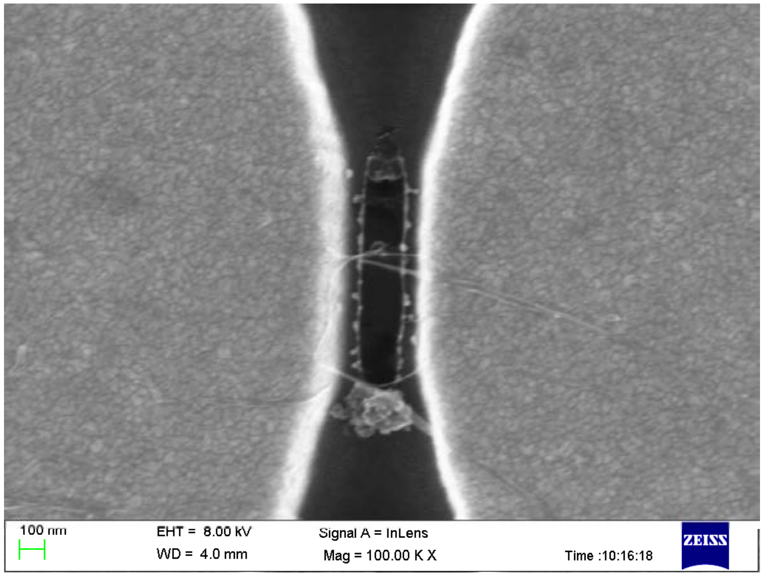


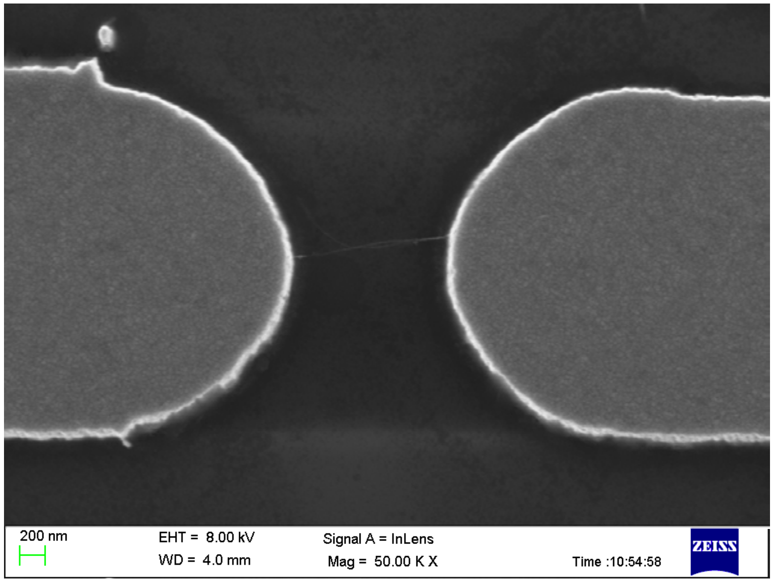
High yield fabrication

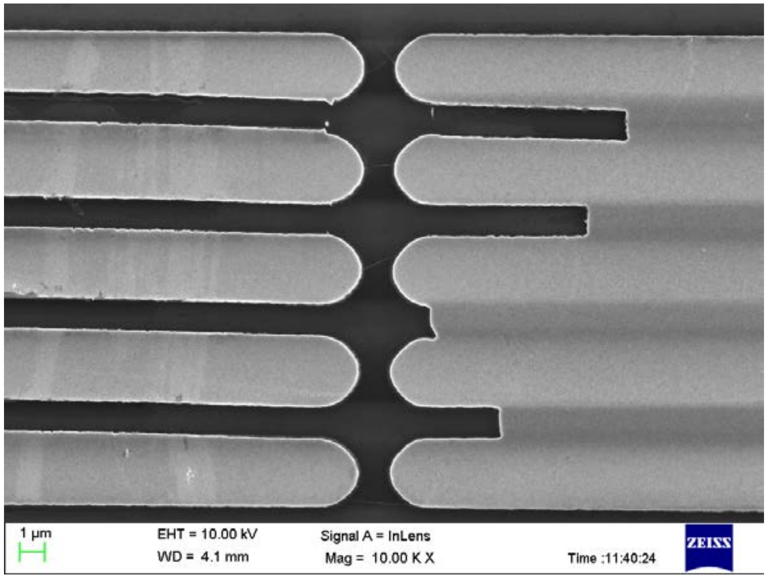
Dielectrophorisis @ sspl

Dielectrophorisis @ sspl

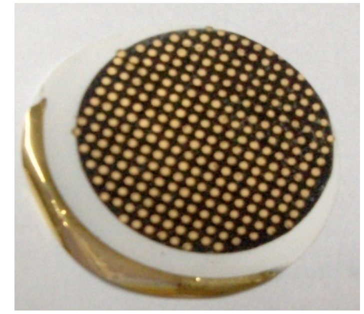


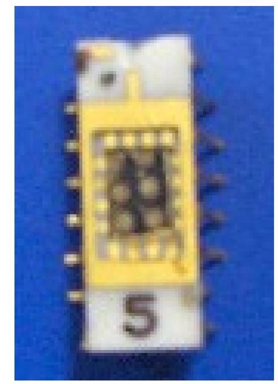


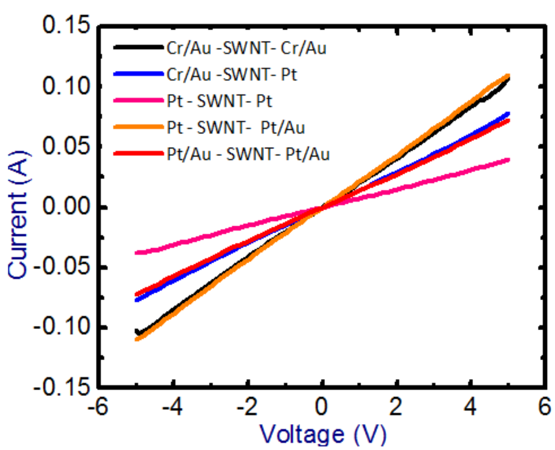


CNT Thin Film Resistor (TFR)

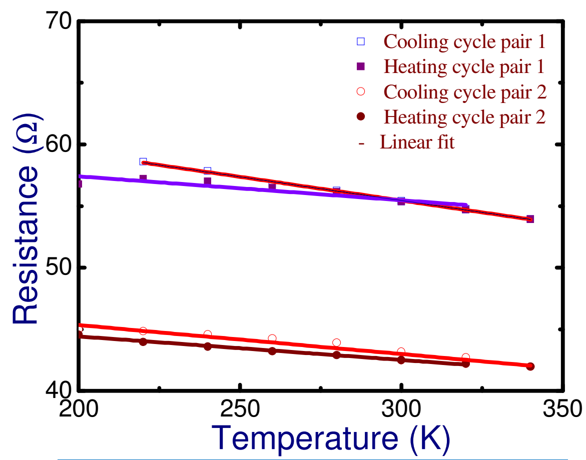
- The maximum, minimum and average TTR:
  - TFR1: 2.02kΩ,0.44kΩand1.12kΩ.
  - TFR2:63Ω,31.68Ωand46.43Ω
- Standard Deviation with location:
  - TFR1 : 46.21% and TFR2: 19.8%
- Contact resistance and sheet resistance:
  - TFR1 0.33kΩ and 0.31kΩ/□.
  - TFR2: 14.48Ω and 10.2Ω/□.
- Observed several types of regions of non-uniformity between the contacts:
  - Well connected CNT-sheet,
  - Partially connected CNT-sheet
  - Missing CNT-sheet



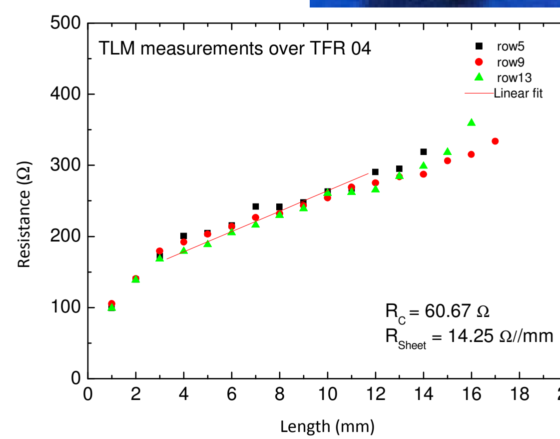




Comparison of IV characteristics of all metal-SWNT-metal contacts

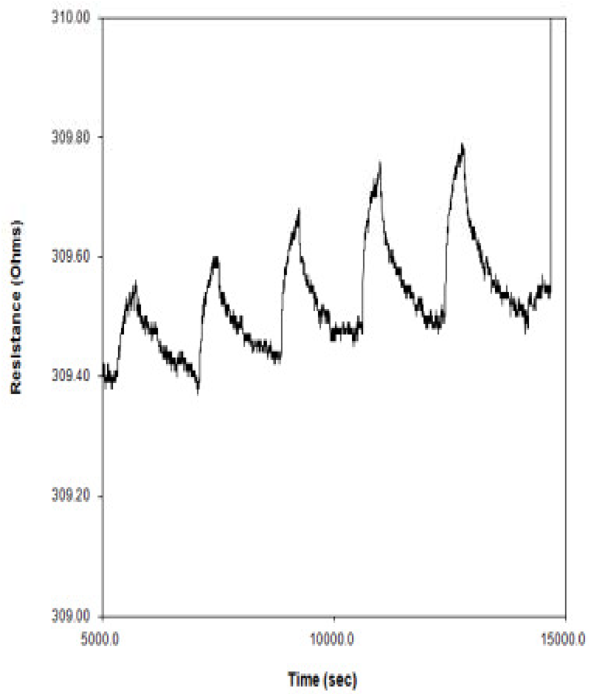


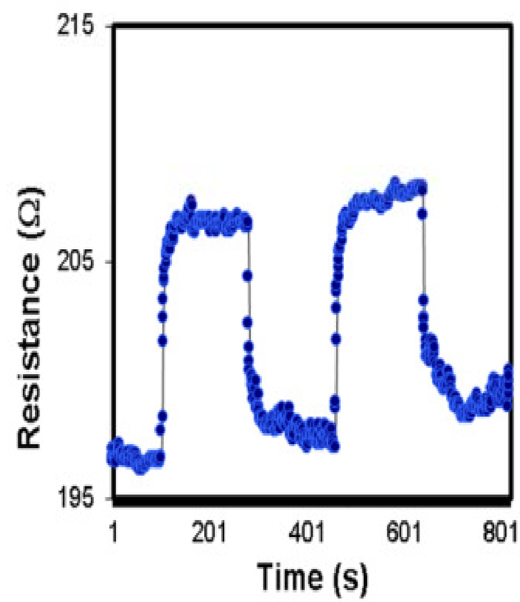
Variations in resistance of the SWNT with Temperature



- ❑ Contact Resistance :~ 60.67 Ω
- ❑ Sheet Resistance: ~14.25 Ω/mm

Response of CNT-TFR to NH_3 and ethanol vapors @sspl





Challenges

- No clear path is seen for extending CMOS (complementary metal oxide semiconductor) technology beyond the roadmap horizon of 2020, when devices will have a physical gate length of only 6 nm.
  - A transition to an alternative technology is needed before 2020 because of the time and energy needed to replace CMOS. The technology can not be replaced abruptly.
- Nanotechnology will pose many ethical and societal questions; these will need to be addressed.
- The skilled work force required to continue the exponential increase in technology is lagging. More people need to be trained in science and technology.

Thank you

Properties and applications

<u>**Properties**</u>

***Mechanical*: highest Young's modulus, highest tensile strength**
***Thermal*: highest thermal conductivity**
***Electrical*: ballistic transport in metallic tubes,highest carrier mobility in semiconductor tubes**

<u>**Applications:**</u>

Carbon nanotube composites
Electrochemical devices
Hydrogen storage
Field emission devices
Nanoelectronic devices
Sensors and probes